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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,467	09/29/2003	Eiichi Fukita	67162-024	7946

7590 05/18/2005

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,467	FUKITA ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/671467 filed on 09/29/03.

Claims 1-9 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. (U.S Patent 6393601).

3. As to claim 1, Tanaka et al. teach a logic circuit diagram input device for estimating a layout area based on a logic circuit diagram constituted by a transistor as a minimum unit, comprising: hierarchy developing means for developing logic circuit diagram information having a hierarchical structure to information at a transistor level (see fig 1 and fig 2 col 7 lines 35 to col 8 lines 40); configuration parameter information extracting means for extracting configuration parameter information such as a gate length, a gate width, a drain region area and a source region area which are added to each transistor as a property (see fig 4 and fig 5a-5c col8 lines 53 to col 9 lines 32) ; area calculating means for calculating each transistor area using a transistor area calculation formula for calculating a transistor area from the said configuration parameter information (see fig 14-23 col 12 lines 16 to col 18 lines 29 especially col 12 lines 16 to col 13

lines 49); and layout area estimating means for estimating a layout area by adding all areas of the transistors together (see fig 6 and fig 7 col 9 lines 34 to col 10 lines 50).

4. As to claim 2, Tanaka et al. teach wherein said each transistor area is corrected using an area possession ratio per predefined transistor (see fig 14-23 col 12 lines 16 to col 18 lines 29 especially col 12 lines 16 to col 13 lines 49).

5. As to claim 3, Tanaka et al. teach a logic circuit diagram input device for estimating a layout area based on a logic circuit diagram constituted by a standard cell, comprising: hierarchy developing means for developing logic circuit diagram information having a hierarchical structure to information at a standard cell level (see fig 1 and fig 2 col 7 lines 35 to col 8 lines 40); an each standard cell area holding part for holding each standard cell area according to an instance (see fig 4 and fig 5a-5c col8 lines 53 to col 9 lines 32); area deriving means for deriving said developed each standard cell area according to the instance of the cell based on data of said each standard cell area holding part (see fig 14-23 col 12 lines 16 to col 18 lines 29 especially col 12 lines 16 to col 13 lines 49); and layout area estimating means for estimating the layout area by adding all of the areas of the standard cells (see fig 6 and fig 7 col 9 lines 34 to col 10 lines 50).

6. As to claim 4, Tanaka et al. teach wherein said each standard cell area is corrected using an area possession ratio defined for each kind of the standard cell (see fig 14-23 col 12 lines 16 to col 18 lines 29 especially col 12 lines 16 to col 13 lines 49).

7. As to claim 5, Tanaka et al. teach wiring information extracting means for extracting wiring information from said logic circuit diagram information having the hierarchical structure (see fig 1 and fig 2 col 7 lines 35 to col 8 lines 40); and probable wiring possession area value holding means for holding a probable value of a wiring possession area, which is defined

according to a layout area and the number of cells, wherein the sum of the probable values of the wiring possession areas which were extracted from the probable wiring possession area value holding means per wiring is added to said layout area (see fig 4 and fig 5a-5c and fig 9 col8 lines 53 to col 9 lines 32 col 10 lines 56 to 11 lines 37).

8. As to claim 6, Tanaka et al. teach each block area wiring capacity of holding part for holding a probable wiring capacity value defined according to a layout area and the number probable wiring capacity value extracting means for extracting probable wiring capacity value from said each block area wiring capacity holding part per wiring (see fig 4 and fig 5a-5c and fig 9 col8 lines 53 to col 9 lines 32 col 10 lines 56 to 11 lines 37).

9. As to claim 7, Tanaka et al. teach wherein information of said probable wiring capacity value is added to wiring data on the logic circuit diagram constituted by a standard cell as a property or an element (see fig 4 and fig 5a-5c and fig 9 col8 lines 53 to col 9 lines 32 col 10 lines 56 to 11 lines 37).

10. As to claim 8, Tanaka et al. teach wherein further detailed physical information such as a maximum gate width, a unit resistance value, a unit capacity value or the like is added other than configuration parameter such as a gate length, a gate width, a drain region area and source region area which were added to a transistor element as a property (see fig 4 and fig 5a-5c col8 lines 53 to col 9 lines 32).

11. As to claim 9, Tanaka et al. teach wherein an area possession ratio is set on higher level of block in stead of an area possession ratio set per transistor (see fig 14-23 col 12 lines 16 to col 18 lines 29 especially col 12 lines 16 to col 13 lines 49).

12. As to claim 10, Tanaka et al. teach wherein each cell, a block area and the number of basic cells (BC) which were estimated by the device are provided to a layout designing apparatus as an input file (see fig 4 and fig 5a-5c and fig 9 col8 lines 53 to col 9 lines 32 col 10 lines 56 to 11 lines 37 and background).

13. As to claim 11, Tanaka et al. teach wherein each cell, a block area and the number of basic cells (BC) which were estimated by the device are stored in each instance element on a logic circuit diagram as a property (see fig 6 and fig 7 col 9 lines 34 to col 10 lines 50).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-1908 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art unit 2825
September 4, 2004

Thuan
THUAN DO
Primary examiner
05/16/2005